

	Type	Ref #	Hits	Search Text
1	BRS	S145	945	(memory adj controller) same design
2	BRS	S146	22	(memory adj controller) same design same asic
3	BRS	S147	0	((memory adj controller) same design same asic) and CAD
4	BRS	S148	0	((memory adj controller) same design same asic) and CAD
5	BRS	S149	1	((memory adj controller) same design same asic) and Internet
6	BRS	S150	0	((memory adj controller) and design).ti.
7	BRS	S151	43	(memory adj controller) and 703/27.ccls.
8	BRS	S152	10	(design same (memory adj controller)) and 703/27.ccls.
9	BRS	S153	373	(ASIC) same interface same configuration
10	BRS	S154	17	((ASIC) same interface same configuration) and CAD
11	BRS	S155	19	((ASIC) same interface same configuration) and CAD
12	BRS	S156	207	((ASIC) same interface same configuration) and (user same select\$)
13	BRS	S157	518	((ASIC) same interface same configuration) and (user adj select\$)
14	BRS	S158	72	((ASIC) same interface same configuration) and (user adj select\$)
15	BRS	S159	11	((ASIC) same interface same configuration) and (user adj selection)
16	BRS	S160	11	((ASIC) same interface same configuration) and (user adj selection) and memory
17	BRS	S161	5	((ASIC) same interface same configuration) and (user adj selection) and memory and controller
18	BRS	S162	18	((ASIC) same interface same configuration) and CAD and user
19	BRS	S163	12	((ASIC) same interface same configuration) and (CAD same user)
20	BRS	S164	0	((ASIC) same interface same configuration) and (CAD same user) and (memory near design)
21	BRS	S165	1	((ASIC) same interface same configuration) and (CAD same user) and (memory near controller)
22	BRS	S166	71	(memory adj controller adj design)
23	BRS	S167	74	(memory adj controller adj design)
24	BRS	S168	2	(memory adj controller adj design) and (ASIC same configuration)
25	BRS	S169	187	(ASIC same CAD)
26	BRS	S170	62	(ASIC same CAD) and (CAD same user)
27	BRS	S171	0	(ASIC same CAD) and (CAD same user) and (memory adj design)
28	BRS	S172	1	(ASIC same CAD) and (CAD same user) and (memory adj controller)
29	BRS	S173	267	(CAD same user same selection)
30	BRS	S174	24	(CAD same user same selection) and (CAD same ASIC)
31	BRS	S175	462	703/27.CCLS.
32	BRS	S176	454	711/171.ccls.
33	BRS	S177	15	711/171.ccls. and (controller same design)
34	BRS	S178	1	711/171.ccls. and (controller adj design)
35	BRS	S179	8	711/171.ccls. and (memory same controller same design)
36	BRS	S180	42	(memory adj controller) and (memory adj interface) and (CAD)

37	BRS	S181	42	(memory adj controller) and (memory adj interface) and (CAD)
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37	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:50		
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	Type	Ref #	Hits	Search Text
38	BRS	S182	0	(memory adj controller) and (memory adj interface) and (design adj file)
39	BRS	S183	521	(memory adj controller) and (memory adj interface) and ASIC
40	BRS	S184	212	(memory adj controller) same (memory adj interface) and ASIC
41	BRS	S185	44	(memory adj controller) same (memory adj interface) same ASIC
42	BRS	S186	0	(memory adj controller) same (memory adj interface) same ASIC same CAD
43	BRS	S187	0	(memory adj controller) same (memory adj interface) same ASIC near CAD
44	BRS	S188	0	((memory adj controller) same (memory adj interface) same ASIC) near CAD
45	BRS	S189	0	((memory adj controller) same (memory adj interface) same ASIC) and CAD
46	BRS	S190	0	((memory adj controller) same (memory adj interface) same ASIC) and CAD
47	BRS	S191	15	((memory adj controller) same (CAD))
48	BRS	S192	5	((memory adj controller) same (CAD)) and (interface same memory)
49	BRS	S193	5	((memory adj controller) same (CAD)) and (interface same memory same controller)
50	BRS	S194	4	((memory adj controller) same (CAD)) and (interface same memory same controller) and design
51	BRS	S195	0	((memory adj controller) same (CAD)) and (interface same memory same controller) and (design near controller)
52	BRS	S196	2	((memory adj controller) same (CAD)) and (interface same memory same controller) and (design same controller)
53	BRS	S197	3424	(memory adj controller).ti.
54	BRS	S198	5	((memory adj controller) and design).ti.
55	BRS	S199	72	((ASIC) same interface same configuration) and (user adj select\$)
56	BRS	S200	15	((ASIC) same interface same configuration) and (user adj select\$) and (memory adj controller)
57	BRS	S201	1	((ASIC) same interface same configuration) and (user adj select\$) and (memory adj controller) and (design same ASIC)
58	BRS	S203	0	(user adj select\$) same design same ASIC same memory
59	BRS	S204	0	(user adj select\$) same design same ASIC and (memory adj controller)
60	BRS	S205	0	(user adj select\$) same design same ASIC and (memory adj controller)
61	BRS	S206	0	(user adj select\$) same design same ASIC and (controller adj design)
62	BRS	S202	12	(user adj select\$) same design same ASIC

63	BRS	S207	214	(user adj select\$) same design same memory
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63	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:21		
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	DBs	Time Stamp	Comments	Error Definition
38	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:50		
39	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:50		
40	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:50		
41	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:50		
42	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:51		
43	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:51		
44	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:51		
45	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:51		
46	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:51		
47	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:54		
48	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:55		
49	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:56		
50	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:56		
51	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:56		
52	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:57		
53	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:57		
54	USPAT; EPO; DERWENT; IBM_TDB	2005/12/21 10:57		
55	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:15		
56	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:15		
57	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:17		
58	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:17		
59	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:18		
60	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:18		
61	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:18		
62	USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/12/21 11:21		

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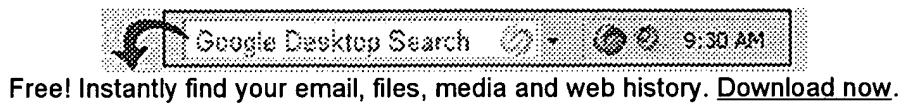
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